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Switching of Three Phase Cascade Multilevel Inverter Fed Induction Motor Drive

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Abstract: *Multilevel inverters have an attracted a great deal of attenuation in medium voltage and high power application Due to their lower switching losses, EMI, high efficiency. This paper proposes to Cascade H bridge multilevel inverter to reduced total harmonic Distortion by increase the output voltage level. The control system of this model is designed using PI controller to increase or decrease the voltage level of inverter in order to achieve the desired speed of induction motor fed through multilevel inverter. Hence the paper mainly focused on 11 level and 13 level three phase cascade H-bridge multilevel inverter. The result shows that the proposed method evaluate three phase cascaded multilevel inverter effectively minimizes a large number of specific harmonics and reduced switching loss , the output voltage in addition of very low total harmonic distortion for 11 level and 13 level inverter.*

Keywords*—Cascaded Multi level inverter (CHMLI), Total Harmonic Distortion (THD), Multi carrier Phase opposition dissposition (POD).*

1. INTRODUCTION

Due to high efficiency with low switching frequency control method in the last few years, the necessity of increasing the power quality enhancement in industry has sustained the continuous development of multilevel inverters. The multilevel inverters improve the AC power quality by performing the power conversion in small voltage steps resulted in lower harmonics. The output voltage on the AC side can take many discrete levels of equal magnitude. The harmonic content of this output voltage waveform is greatly reduced, a smaller filter size and a lower EMI, if compared with a two level voltage waveform. There are many topologies for multi-level inverters have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H bridge structures. One aspect which sets the cascaded H Bridge apart from other multi-level inverters is the
Capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion amongst.

This paper presents a three-phase 11 level and 13 level cascade H-bridge inverter fed induction motor drive with a multi carrier Pulse width modulated control scheme. It is ma-
-in reason to simplicity of control and a cascade multilevel inverter is built to synthesize a desired AC voltage from several levels of DC voltages. Though the cascaded has the Drawback to need separate dc sources the problem of the dc link voltage unbalancing does not occur, thus easily defined to many level. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors. The result shows that the proposed method effectively minimizes a large number of specific harmonics, and the output voltage result in very low total harmonic distortion and switching frequency.
This paper highlights the control system of this model is designed using PI controller to increase or decrease the voltage level of inverter in order to achieve the desired speed of induction motor fed through multilevel inverter with reduced total harmonic distortion . The modeling of in this paper highlights significance of an eleven level and thirteen level cascaded multilevel inverter.

2. CASCADED MULTILEVEL INVERTERS

A. Basic Structure and Operating Principle

The general function of cascade multilevel inverter is the similar as that of two level inverters. The cascaded-inverter with SDCSs synthesizes a desired voltage from several independent Sources of dc voltages, which may be obtained from batteries, Fuel cells, or solar cells, etc. The output ac terminal voltages of different level inverters are connected in series. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors. The cascaded multilevel inverter configuration recently becomes very popular in AC power supply and adjustable speed drive applications. Figure 1 shows a single-phase

structure of an 11-level cascade inverter. Each DCS is connected to a single phase full bridge, or H-bridge inverter.

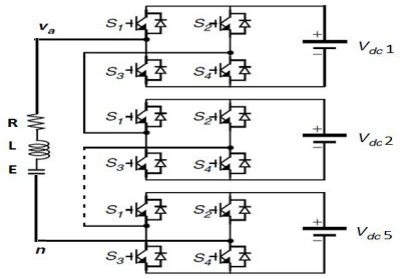

Figure 1. Single-phase structure of a 11 level cascaded H bridges inverter

Each inverter level can generate three different voltage outputs, *+Vdc*, 0, and *-Vdc*, by connecting the dc source to the ac output by different combinations of the four switches, *SI*, *S2*, *S3*,and *S4*,. To obtain *+Vdc*, switches *SI* and *S4* are turned on. Turning on switches *S2* and *S3* yields *-Vdc*. By turning on *SI* and *S2*, or *S3* and *S4*, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels *m* in a cascade inverter is defined by m = 2s+l, where s is the number of separate dc sources (photovoltaic modules or fuel cells). The proposed method has been designed an eleven level and thirteen level cascade multilevel inverter which has five and six respectively single phase full bridge inverter connected in series.

For an eleven level cascade multilevel inverter used five SDCSs and five full bridges is shown in above fig. the phase voltage Van is given by

Van = Va1 + Va2 + Va3 + Va4 + Va5 ……Eq (1)

The Fourier Transform for this waveform follows

V (wt) =4Vdc/π Σn [cos (nθ1) + cos (nθ2) +……
.... cos (nθs)] xsin (nwt)/n ……Eq(2)

Where n=1, 3, 5, 7

When normalized with respect to Vdc then the magnitude of the Fourier coefficients are as follows

H (n) =4V/πn Σn [cos (nθ1) + cos (nθ2) +……
….cos (nθs)] ……Eq(3)

Where n=1, 3, 5, 7…….

B. Modulation Scheme

In this paper, control technique of sinusoidal pulse width modulation (SPWM) strategy employed. This is the phase opposition disposition method of Level Shifted Multicarrier Modulation technique. In this method the no of carrier triangular or rectangular wave are compared with sinusoidal reference modulating signal .The carrier waveforms are in all phase above and below the zero reference value. However there is180 degrees phase shift between the ones above and below zero respectively.

The switching for all the switches is decided by the intersection of the modulating sinusoidal signal on the all carriers' signals. The proposed thirteen level inverter one modulating signal and ten carrier wave necessary for each phase of the inverter as shown in below figure 3.

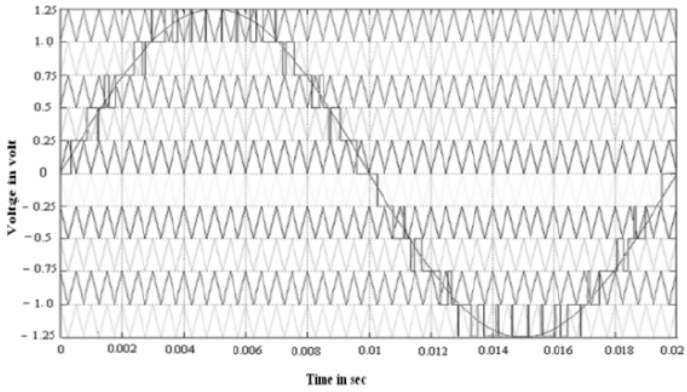

Figure 2. Modulation Scheme of eleven level inverter

Each phase modulating signal is displaced 120 degree from each other. Frequency and amplitude both are same for all the carrier signal while the modulating signal has a frequency and amplitude is Fm and Am respectively. The carrier wave frequency and amplitude is fc and Ac respectively. The fc should be in integer the multiples of fm with three-times. The modulating signals and carrier waves are compared and the output of the comparator defines the output voltage waveform. Five carrier wave are placed above the zero reference signals and five opposite phase carrier waves are placed below the zero reference signals. In the positive half cycle the comparator output will have the high value if the amplitude of the modulating signal is greater than that of carrier wave and zero otherwise. Same process is repeated for the negative half cycle of the modulating signal. If the modulating signal is lower than the carrier wave, the output of the comparator is high and zero otherwise.

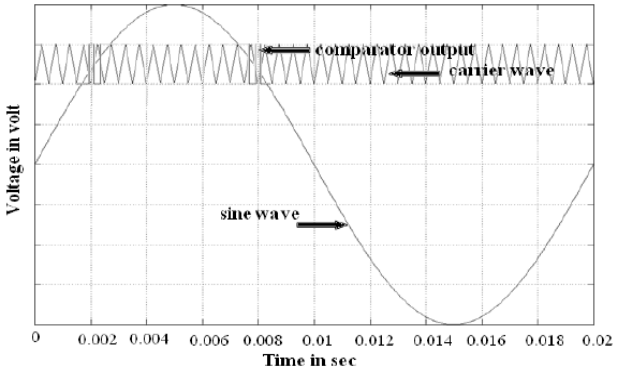

Figure 3. Sinusoidal and Carrier Wave Comparison

C. Induction Motor Drive

The induction motor drive means to control the speed of induction motor. By using PI controller the speed of induction motor is controlled. PI controller to increase or decrease the voltage level of inverter in order to achieve the desired speed of induction motor fed through multilevel inverter .The output of multilevel inverter is given to the induction motor then the desired speed of the induction motor is achieve by changing the separate input dc voltage . This is done by using the controlled DC voltage in which PI controller change the input DC voltage .the speed of the motor is directly depends upon the voltage .so this is the closed loop speed control of induction motor. The desired speed can be achieved by changing the output voltage level of the inverter.

3. IMULATION INVESTIGATION

A. Simulation Model and CMLI Discussion

Three phase MATLAB / SIMULINK simulation model of cascade multilevel inverter as show in figure 4. It has two systems one is inverter and other is fed induction motor drive.

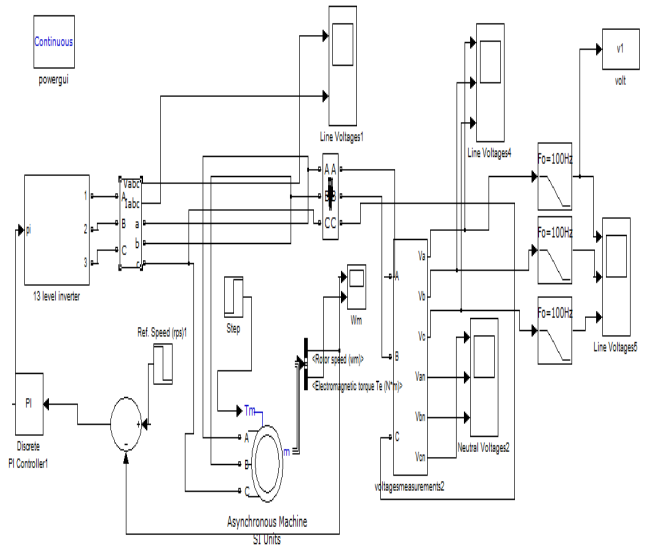

Figure 4. Simulation model of three phase cascade 13 level inverter fed induction motor drive

Twelve switching pulse are required for 13 level cascade inverter. In figure 5 .the simulation model of switching pattern contain twelve carrier waves and one sinusoidal wave and a relational operator. Each comparator produces the sequence of switching pulse for semiconductor switching. The thirteen-level cascaded multilevel inverter control circuits produce switching pulses for Sj switches where s=1 to 12. The sequence of the switching pulse turn on switching devices, and the cascade multilevel inverter produce thirteen level output voltage. The modulation scheme for thirteen level inverter is shown in figure 5.

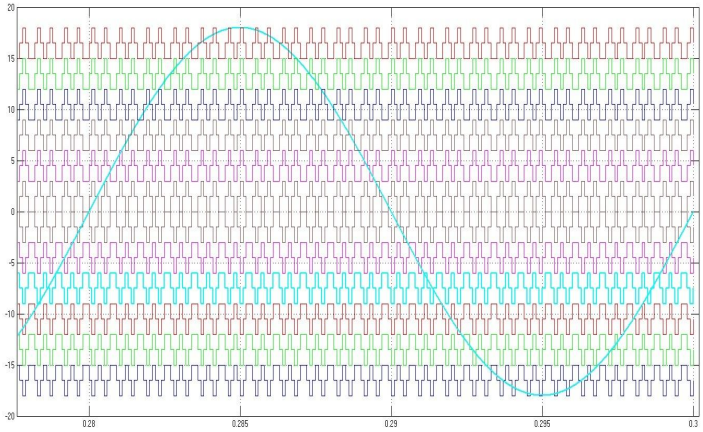

Figure 5. Modulation Scheme for 13 level inverter

B. SIMULATION RESULTS

The eleven-level cascaded and thirteen level cascade multilevel inverters have been simulated using MATLAB; the inverter is supplying a balanced three phase voltage to induction motor. The cascaded multilevel inverter balanced output the phase voltage is 400V, 50 Hz. The thirteen level inverter devices have been assumed to be nearly ideal for simulation. Inverter output quantities such that output of inverter line voltage and three phase balanced line voltage for eleven levels and thirteen level as shown in below figures 6 and figure 7

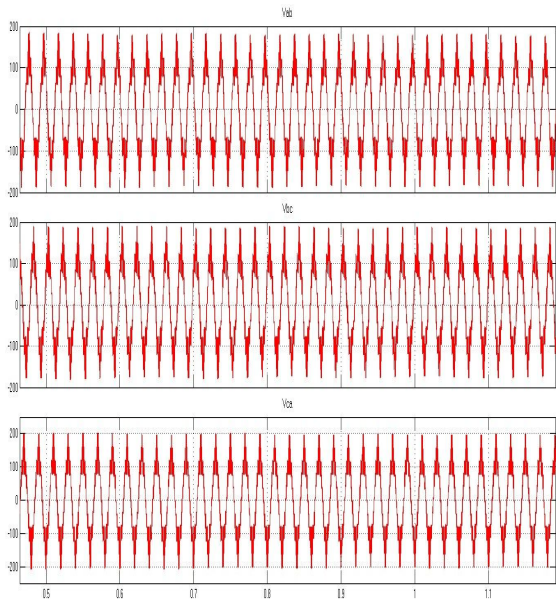

Figure 6. Line voltage of three phase CMLI (without filter)

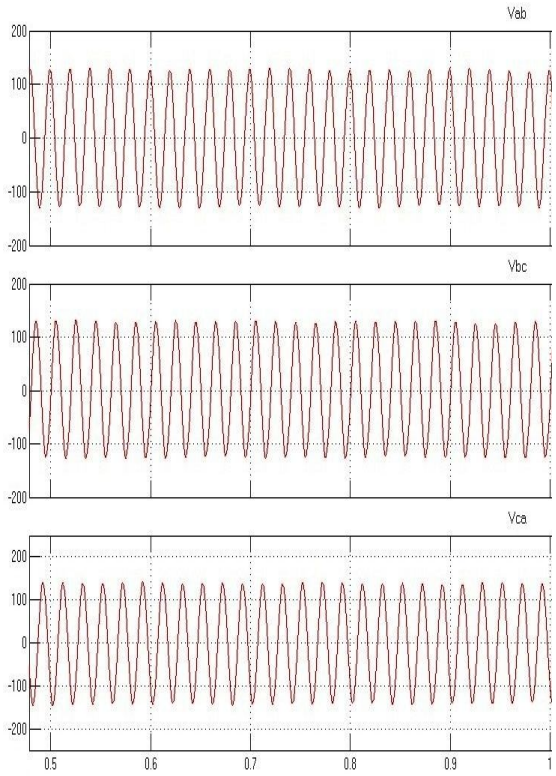

Figure 7. Thirteen Level three phase balanced line voltages (with filter)

There are many advantages of Induction motor due to this it is widely used in industries. The output of 11 and 13 level cascade multilevel inverter is fed to the induction motor to verify the basic performance of inverters like voltage fluctuation, frequency variation, etc. since the induction motor treated as the load to the inverter, if any variation in the performance of the multilevel inverter reflect on the performance of the motor. An eleven level and thirteen level cascade multilevel inverter fed induction motor speed curve results show in figure below. It settles to a constant speed very quickly (after 2 sec). The rotor speed and electromagnetic torque curve is shown in below figure 8.

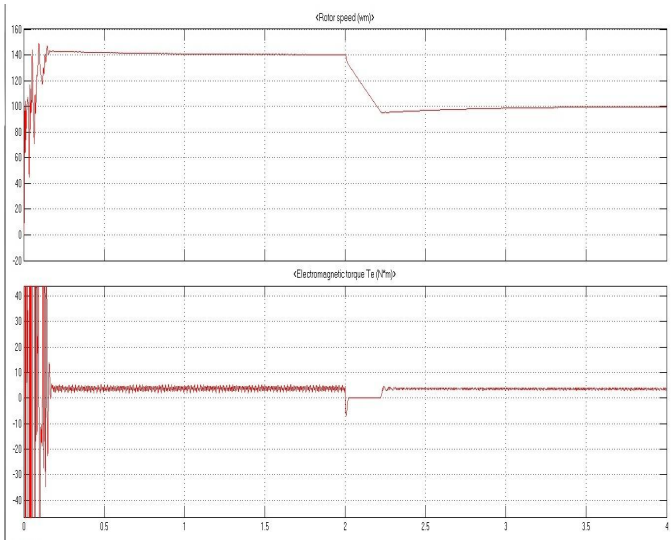

Figure 8. Rotor speed and electromagnetic torque

Total Harmonic Distortion of thirteen level cascade multilevel inverter has 2.44% it illustrated in below figure. The thirteen level cascade multilevel inverter THD value is reduced to the eleven level cascade multilevel inverter.

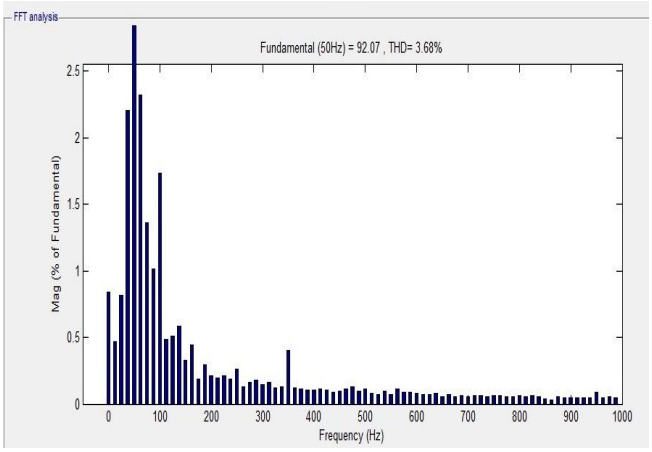

Figure 9. %THD of eleven levels CMLI

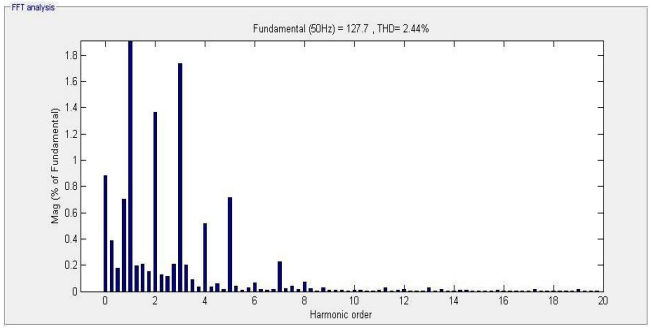

Figure 10. %THD of thirteen levels CMLI

The THD value of nine level, eleven levels and thirteen levels cascade multilevel inverter is given in below table 1-

Table 1. Comparison table of THD %

nine-level (% of THD)	**eleven-level (% of THD)**	**thirteen-level (% of THD)**
13.22	3.68	2.44

4. CONCLUSION

In this paper, some improvements in the way of cascaded multilevel inverter have been proposed the basic structure and operating characteristics of cascaded multilevel inverter have been described by taking an thirteen -level inverter configuration. The thirteen -level cascaded multilevel inverter

Has been illustrating in simulation results by using MATLAB.

Multilevel inverters are used to high power applications and if fed induction motor drive it also controls the speed of induction motor by changing the output voltage level. The

inverter cell is low means the design of the inverter switch pattern is easiest. The technique is used to improve the level of the inverter and extends the design flexibility and reduces the total harmonics distortion.

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